Amendments to the Specification:

Please amend the specification as follows:

Please rewrite the Summary of the Invention (beginning on page 3, line 9) as follows:

According to an aspect of the present invention, there is provided a semiconductor memory device comprising a memory cell array having a plurality of memory cells arranged in rows and columns, the memory cells storing data and being selected according to address signals; and a control circuit, receiving a clock signal and a first control signal, configured to output a plurality of data in synchronism with the clock signal after the first control signal is asserted, output of the data beginning a number of transition (N) of an internal signal (N being a positive integer $\geq$ 2) which responds to the clock signal after the first control signal is asserted, at least one of the data being output at the transition of the internal signal after the output begins.

According to another aspect of the present invention, there is provided a semiconductor memory device comprising a memory cell array having a plurality of memory cells arranged in rows and columns, the memory cells being selected on an address signal; and a control circuit configured to receive a first signal having a first state and a second state, and a second signal having a third state and a fourth state, and configured to output a plurality of data stored in the memory cells responding to the first signal, after a third signal switches N times (N $\geq$ 2, N is a positive integer) between a fifth state and a sixth state in response to the first signal switching between the first state and the second state after the second signal switches between the third state and the fourth state.

~~According to an aspect of the present invention, there is provided a method of accessing a semiconductor device that operates in synchronism with a clock signal, comprising fetching information indicating a memory cell location in a memory cell array in synchronism with the clock signal, determining first data of a plurality of data to be transferred sequentially, decoding the information indicating the memory cell location in the memory cell array and designating the memory cell, receiving data stored in the memory cell designated by the information indicating the memory cell location in the memory cell array in synchronism with the clock signal after a predetermined number of cycles of the clock signal, and outputting a plurality of data stored in the memory cells in synchronism with the clock signal and storing a plurality of input data in the memory cells in synchronism with the clock~~